

FIG. 1

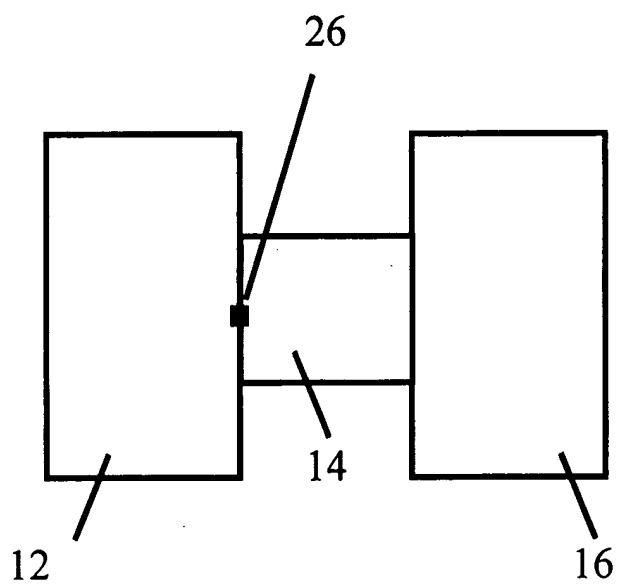


FIG. 2

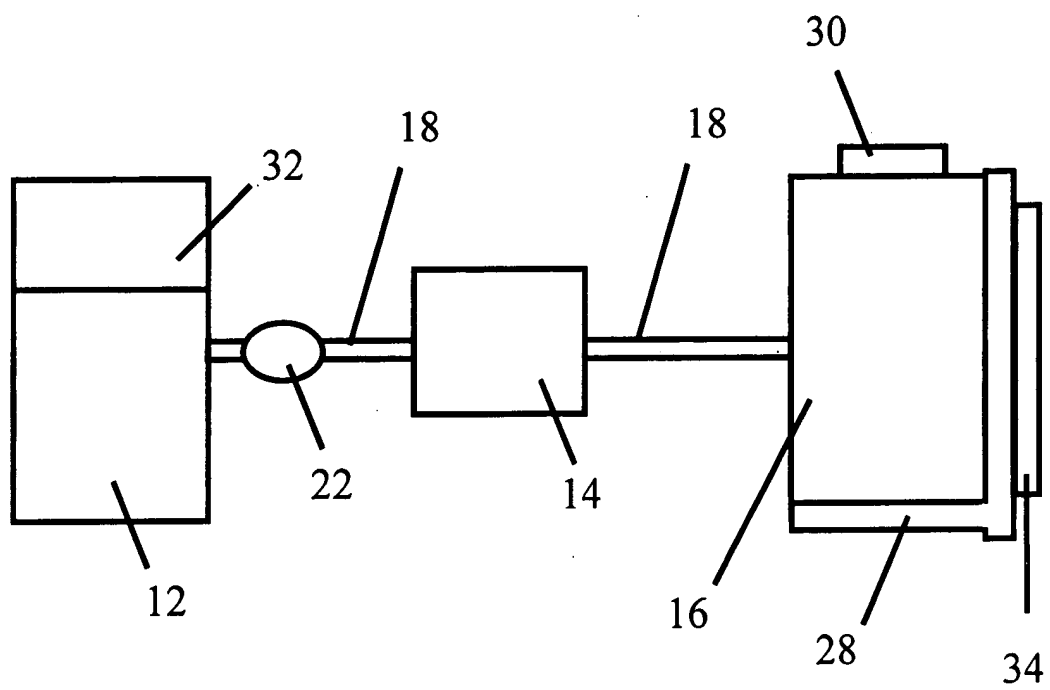


FIG. 3

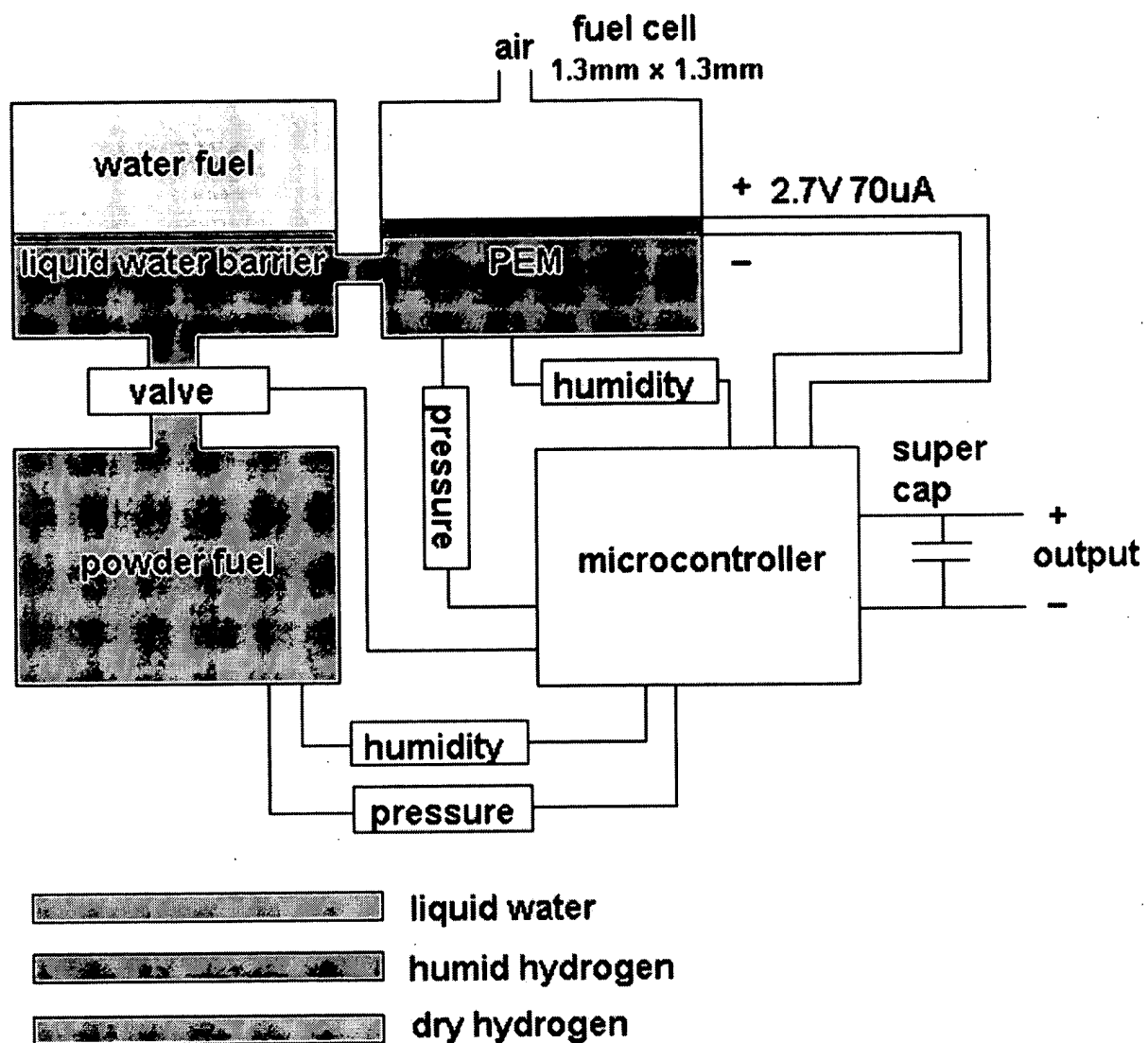


FIG. 4

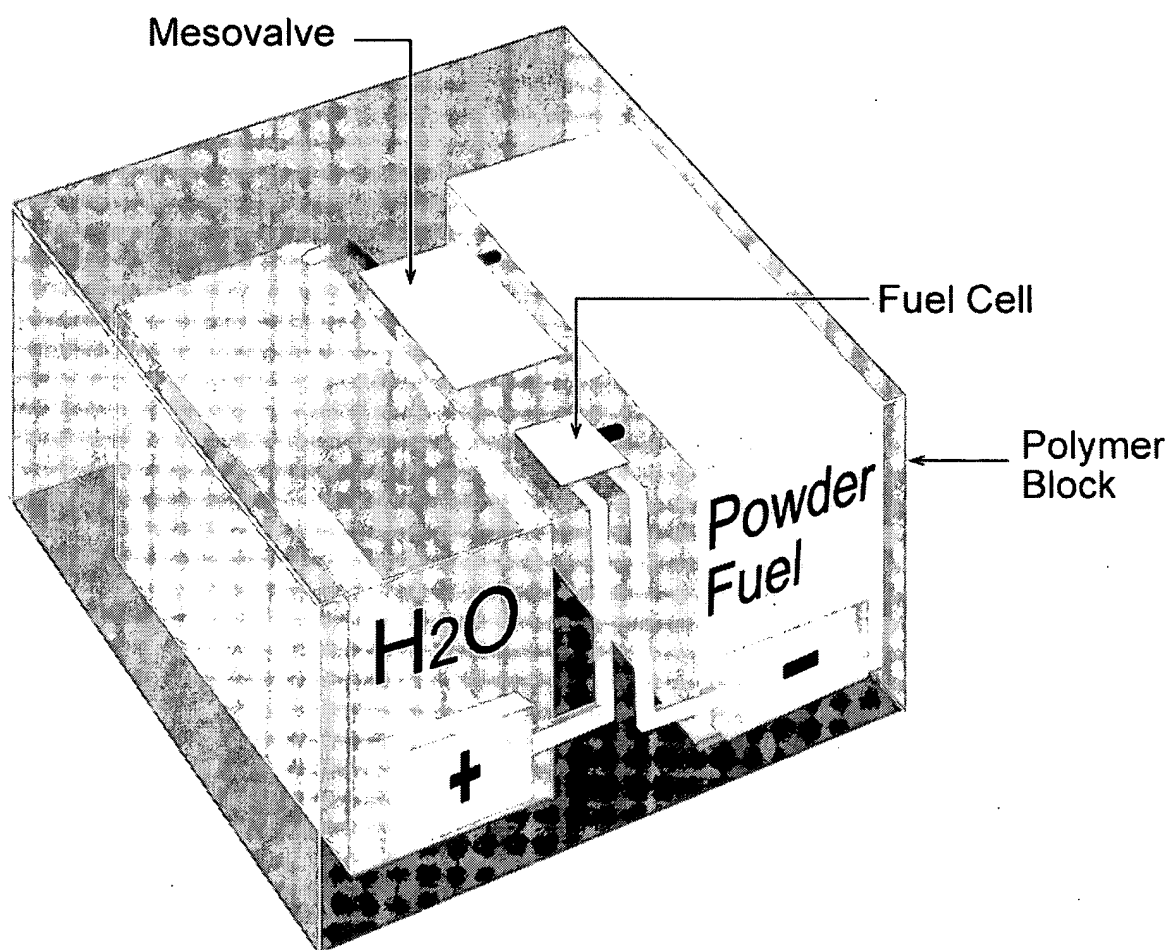


FIG. 5

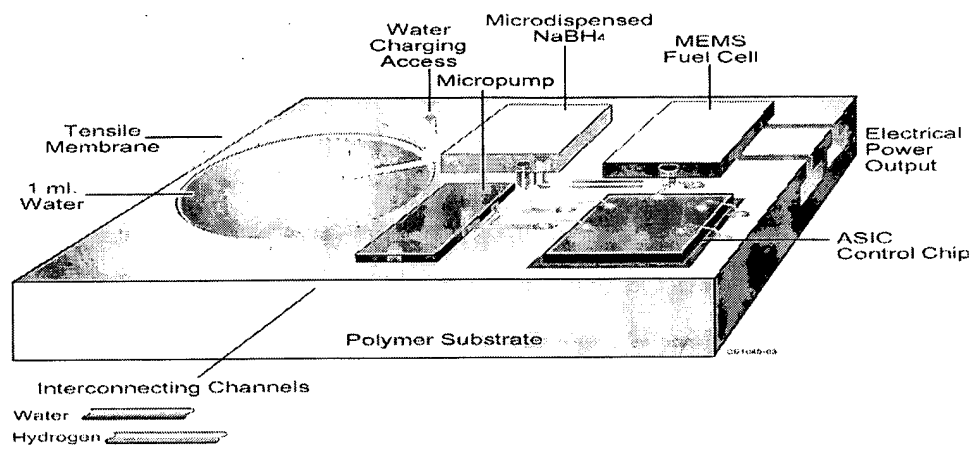


FIG. 6

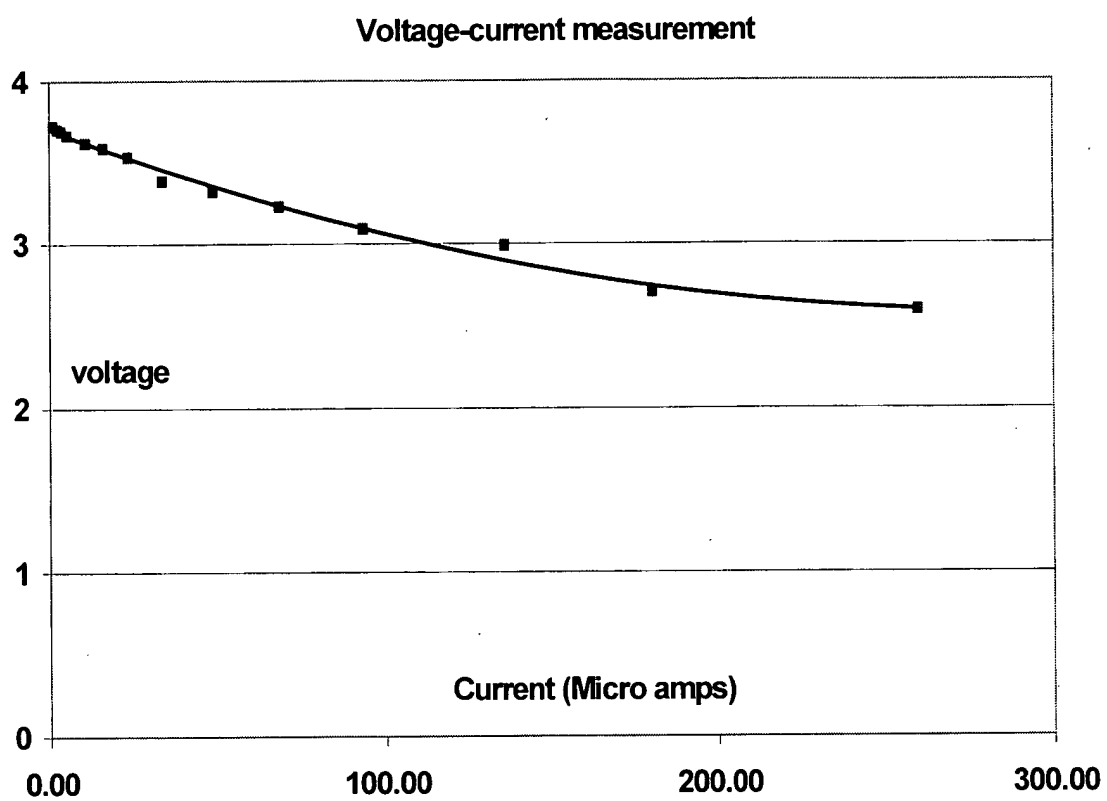
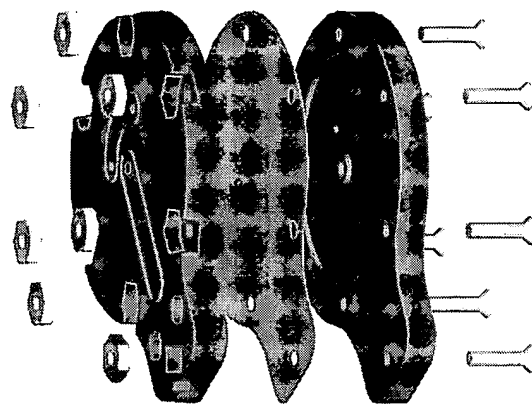


FIG. 7



FIG. 9



ACTIVE PART - BOTTOM PLATE



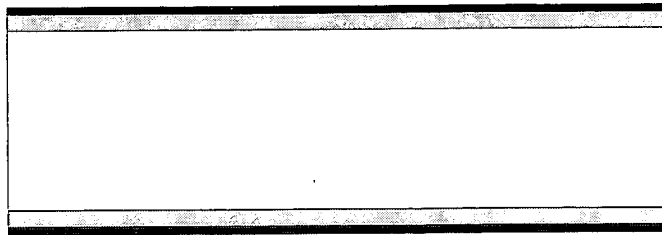


Fig. 10A

*Double polished Si wafer with thick thermal oxide and LPCVD nitride suitable for creating through the wafer etch holes.*

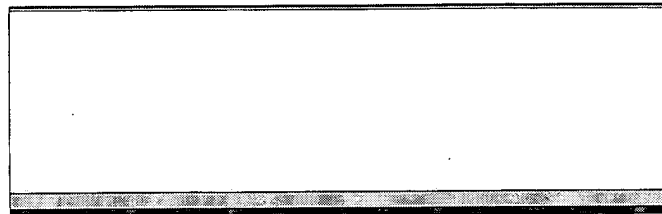


Fig. 10B

*Strip off nitride and oxide from front of wafer, grow thin thermal oxide and bottom bridge dielectric (nitride)*

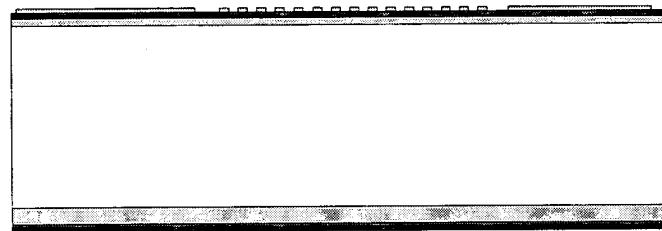


Fig. 10C

*Deposit and pattern lower electrode, such as TiW/Au or Cr/Au.*

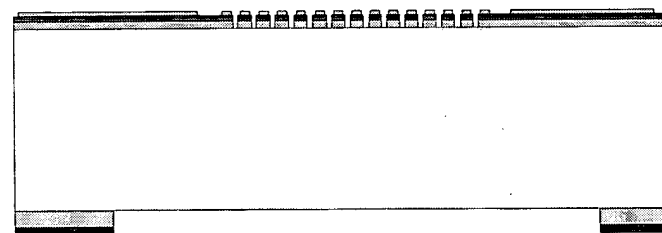


Fig. 10D

*Deposit and pattern lower electrode, such as TiW/Au or Cr/Au.*

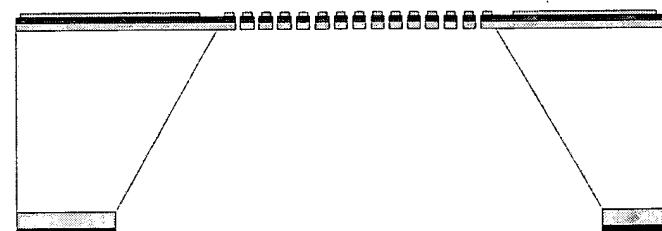


Fig. 10E

*Etch from backside to release diaphragms.*

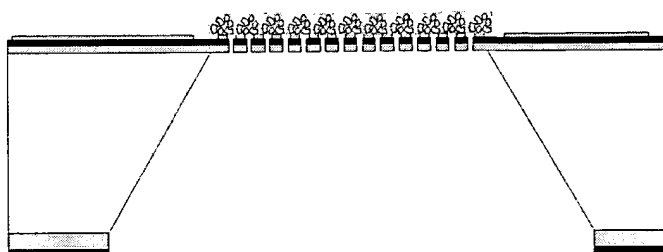


Fig. 10F

*Apply catalytic paste by "doctor blading"*

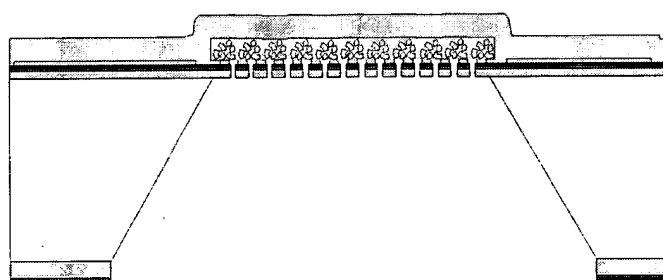


Fig. 10G

*Apply PEM layer such as by spinning.*

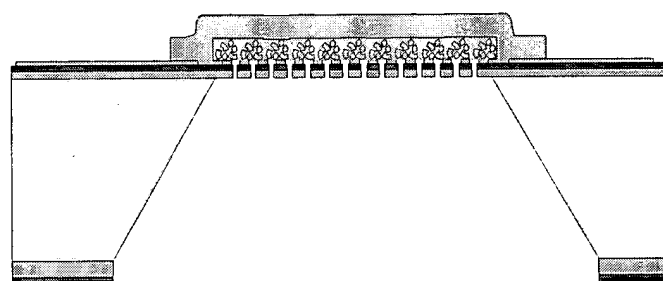


Fig. 10H

*Pattern PEM layer*

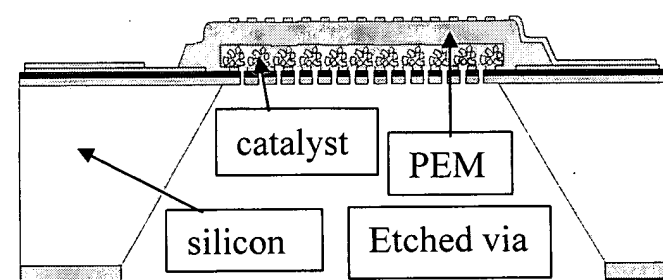


Fig. 10I

*Apply and pattern upper electrode*

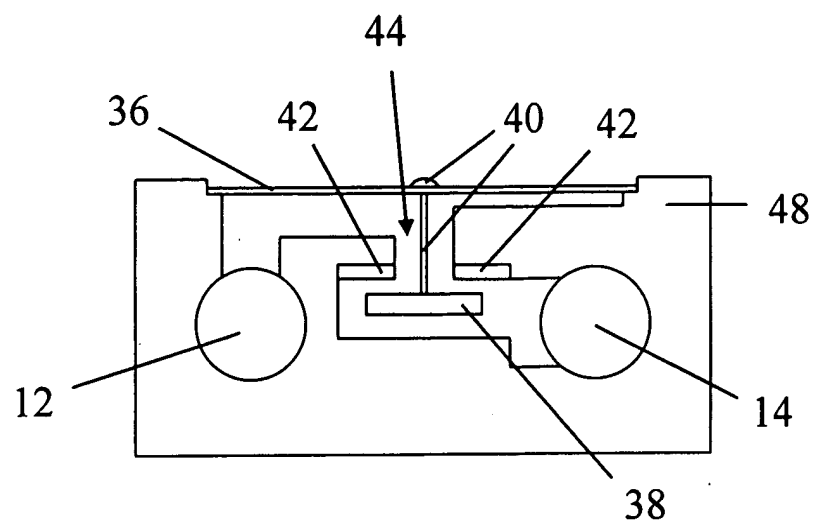


FIG. 11

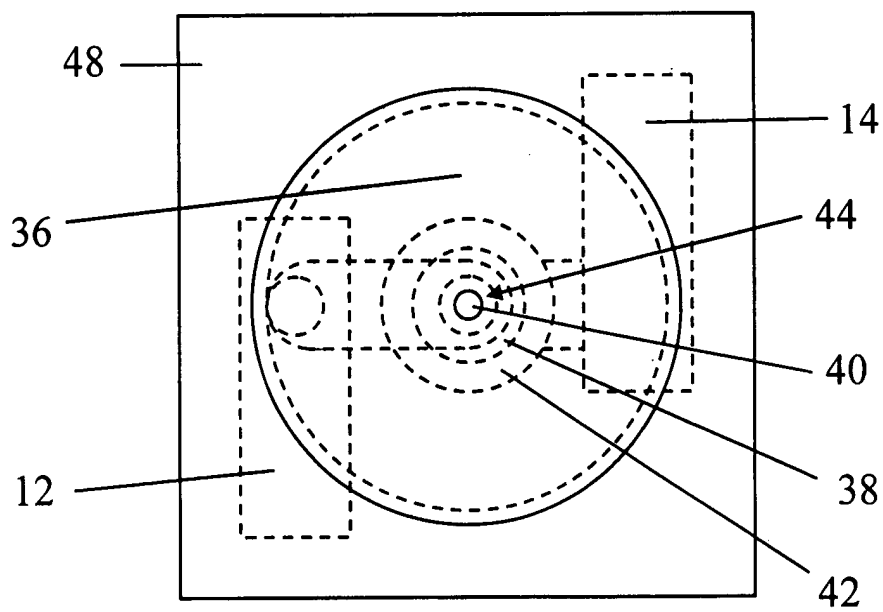


FIG. 12

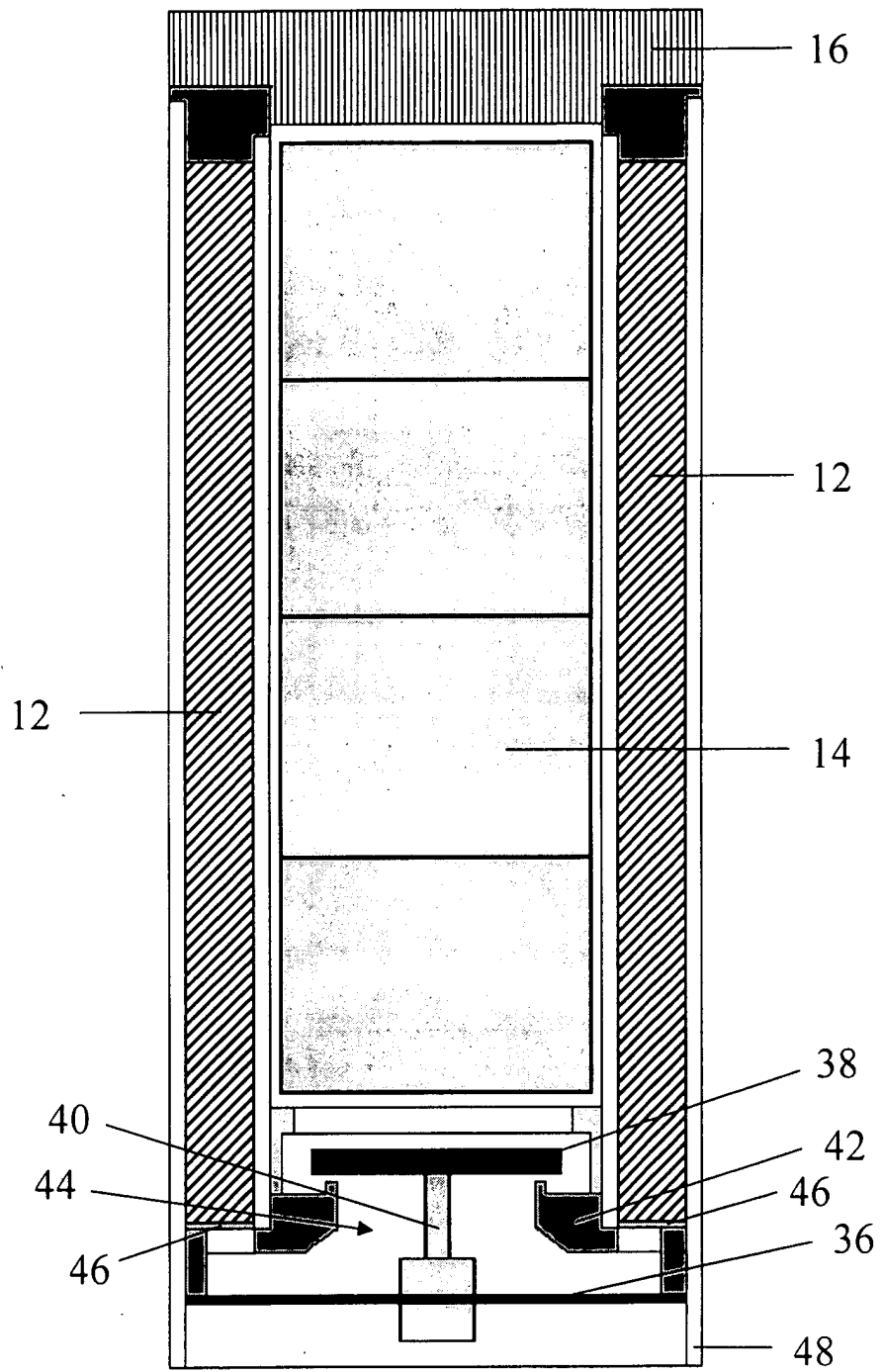


FIG. 13